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Application No.	091827,073	Prepared by	NH	Tracking Number	05914557
Examiner-GAU	Phan-2818	Date	3-29-4	Week Date	03/08/04
		No. of queries	1		JFW

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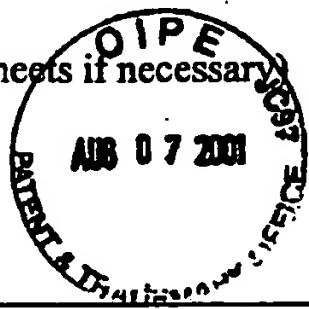
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

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Form PTO-1449 U.S. DEPARTMENT OF COMMERCE
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**LIST OF PRIOR ART
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Atty. Docket No.

Y0R920000587US1 (13958)

Serial No.

09/827,073

RECEIVED

AUG 09 2001

Applicant

Louis L. Hsu et al.

Technology Center 2100

Filing Date

April 5, 2001

Group

U.S. PATENT DOCUMENTS

EXAMINE R INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	"An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D ² RAM)", Yasuhiro Agata et al, 2000 IEEE International Solid-State Circuits Conference, 9 pages.

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.